#8 Amdt (NE) 9.3.02 aps

Docket No. JCLA5285
US App. No. 09/451,135

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : CHIEN-PING HUANG et al.
Application No. : 09/451,135
Filed : November,30,1999
For : BALL GRID ARRAY PACKAGE AND A PACKAGING PROCESS FOR SAME
Examiner : PAREKH, NITIN
Attorney Docket No. : JCLA5285

entered JMcmillan 12/16/02

AMENDMENT AFTER FINAL

FAX COPY RECEIVED
AUG 27 2002
TECHNOLOGY CENTER 2800

Box AF
Assistant Commissioner for Patents
Washington, DC 20231

Don't enter this amendment. AC 12.3.02

Dear Sir:

In response to the Office Action dated June 18, 2002, please enter the following amendments and consider the following remarks:

In the Claims:

Please cancel claims 27, 38, and 40 without prejudice and disclaimer.

Please amend claims 26, 28, 30, 36, and 39 as follows:

26. (Twice amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate;

a stack of metal layers alternating with dielectric layers on the substrate, wherein the metal layers are coupled with one another by a plurality of via plugs in the dielectric layers, the via plugs being placed in alternating manner with respect to one another through the stack, and the metal layers are in a concentric circle arrangement, to reduce the capacitance by reducing the area of the substrate overlapped by the metal layers;

Cont'd

an uppermost metal layer positioned on the stack and electrically connected to the stack, wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer; and

A1

a passivation layer having a bonding pad opening positioned on the uppermost metal layer for externally electric connection.

28. (Twice amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate;

a stack of metal layers alternating with dielectric layers on the substrate, wherein the metal layers are coupled with one another by a plurality of via plugs through the dielectric layers and are placed in a concentric circle arrangement, to reduce the capacitance by reducing the area of the substrate overlapped by the metal layers;

A2

an uppermost metal layer positioned on the stack and electrically connected to the stack; and

a passivation layer having a bonding pad opening on the uppermost metal layer for externally electric connection.

30. (Twice Amended) A low-capacitance bonding pad for a semiconductor device, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region; and

A3

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by a plurality of via plugs through the dielectric layers, wherein the bonding pad is aligned with the doped region and the metal layers are in a concentric circle arrangement to reduce the capacitance by reducing the area of the substrate overlapped by the metal layers.

A4

36. (Once Amended) A semiconductor device, comprising:

a substrate having a well;

Cont'd 84

a doped region formed in the well as a diffusion region;

a bonding pad on the substrate, the bonding pad being comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by a plurality of via plugs through the dielectric layers, wherein the bonding pad is aligned with the doped region, and wherein the metal layers in the stack are in a concentric circle arrangement to reduce the area of the substrate overlapped by the metal layers; and

a semiconductor device under the bonding pad.

39. (Once Amended) A semiconductor device, comprising:

a substrate having a well;

a doped region formed in the well as a diffusion region;

85

a bonding pad on the substrate, the bonding pad comprising a stack of metal layers alternated with dielectric layers and an uppermost metal layer, the metal layers and the uppermost metal layer being electrically connected to one another by means of a plurality of via plugs, wherein the bonding pad is aligned with the doped region; and wherein an area of each metal layer in the stack is smaller than that of the uppermost metal layer, and the metal layers are in a concentric circle arrangement to reduce the area of the substrate overlapped by the metal layers; and

a semiconductor device under the bonding pad.

REMARKS

All pending claims 26-41 were rejected either under 35 U.S.C. 102(b) or under 35 U.S.C. 103(a). Applicant has amended claims 26, 28, 30, 36, and 39 and canceled claims 27, 33, and 40. No new matter adds through the amendments. For the reasons discussed below, the remaining claims are patentable over the cited references. Withdrawal of the rejections is requested.

Claim Rejections- under 35 U.S.C. 102(b) or 35 U.S.C. 103(a):

Claim 26 was rejection under 35 U.S.C. 102(b) as being clearly anticipated by Oku et al. (U.S. 5,394,013).

Claims 27-41 were rejected either under 35 U.S.C. 103(a) as being unpatentable over Oku in view of Yuan (U.S. 5,838,043).

Applicant has amended claims 26, 28, 30, 36, and 39 to recite that *the metal layers are in a concentric circle arrangement to reduce the capacitance by reducing the area of the substrate overlapped by the metal layers*, or similar limitation, as suggested by Examiner Alonzo Chambliss. None of the cited references teach or suggest these features. Thus, the amended claims 26, 28, 30, 36, and 39, as well as their dependent claims 29, 31, 32, 34, 35, 37, 38, and 41 are patentable over the cited prior art.

Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that the remaining claims are now in condition for allowance and allowance of this application is earnestly solicited.

Respectively submitted

Date: 8/27/2002

Jiawei Huang
Registration No. 43,330

J.C. Patents
4 Venture, Suite 250
Irvine, CA 92618
(949) 660-0761